cont. thin inter-polysilicon dielectric 158 at a pointed corner of floating gate 153. This is shown by the arrow E in Fig. 1B.--

IN THE CLAIMS:

Please **cancel** claims 19 and 20 without prejudice, **amend** claims 1, 6, 7, 9, 26, 27, and 28, and **add** new claims 37-49 as follows.

1. (Amended) A cell structure comprising:

a first junction and a second junction separated by a channel region, the first and second junctions being in a body region, the separation between the first and second junctions defining a cell channel length extending horizontally, each of the first and second junctions having a vertically-extending width, a horizontally-extending length, and a depth;

first and second floating gates over the channel region; and

a select-gate having a portion between the first and second floating gates, the select-gate also extending over at least a portion of each of the two floating gates and extending across the entire length of each of the first and second junctions, and the select gate being separated from the first and second floating gates only by an insulating layer.

6. (Amended) The cell structure of Claim 5 wherein the insulating layer is thinnest between the sharp edge of each of the two floating gates and the select-gate.

7. (Amended) The cell structure of Claim 1 wherein each of the first and second floating gates has a vertically-extending width, a horizontally-extending length, and a depth, the select-gate extending across the entire length of each of the first and second floating gates.

9. (Amended) The cell structure of Claim 1 wherein each of the first and second floating gates stores one bit of information.

Please cancel claims 19 and 20.

26. (Amended) The cell structure of Claim 1 in combination with other similar cell structures forming a virtual ground array of rows and columns of cells, the cells along each row

being serially connected, the select-gates of the cells along each row being connected together forming a plurality of horizontally-extending select-gate lines, the first junction of cells along each column of cells being connected together forming a first plurality of vertically-extending bitlines, and the second junction of the cells along each column of cells being connected together forming a second plurality of vertically-extending bitlines.

27. (Amended) The cell structure of Claim 1 wherein the insulating layer has a weak region so that electrons can tunnel from the first and second floating gates to the select-gate.

28. (Amended) A memory array comprising:

a plurality of cells arranged to form rows and columns of cells, each cell comprising:

a first junction and a second junction separated by a channel region, the first and second junctions being in a body region, the separation between the first and second junctions defining a cell channel length extending horizontally, each of the first and second junctions having a vertically-extending width, a horizontally-extending length, and a depth;

a first floating gate and second floating gate, the first floating gate extending over a first portion of the channel region and over a portion of the first junction, and the second floating gate extending over a second portion of the channel region and over a portion of the second junction;

a select-gate extending over the two floating gates and extending across the entire length of each of the first and second junctions, the select-gate having a portion between the first and second floating gates, the portion of the select-gate extending over a third portion of the channel region between the first and second channel portions, wherein the first, second, and third portions of the channel region do not overlap and together form the entire channel region;

an inter-polysilicon dielectric layer insulating the first and second floating gates from the select-gate, the select gate being separated from the first and second floating gates only by said inter-polysilicon dielectric layer; and

a gate-dielectric layer insulating the first and second floating gates and the portion of the select-gate from the underlying channel region and the first and second junctions,

wherein the cells are serially connected along each row, the select-gates of the cells along each row being connected together forming a plurality of horizontally-extending select-gate lines, the first junction of the cells along each column of cells being connected together forming a first plurality of vertically-extending bitlines, and the second junction of the cells along each column being connected together forming a second plurality of vertically-extending bitlines.

The following new Claims 37-49 have been added.

37. (New) The memory array of Claim 28 wherein each of the first and second floating gates has at least one slanted surface forming a sharp edge so that the inter-polysilicon dielectric layer is thinnest between the sharp edge of each of the two floating gates and the select-gate.

38. (New) A method of operating a memory cell having first and second junctions in a body region, the first and second junctions being separated by a channel region, the separation between the first and second junctions defining a cell channel length extending horizontally, each of the first and second junctions having a vertically-extending width, a horizontally-extending length, and a depth, the memory cell further having first and second floating gates extending over the channel region, and a select-gate extending over the first and second floating gates and extending across the entire length of each of the first and second junctions, the select gate being separated from the first and second floating gates only by an insulating layer, the method comprising:

storing a first bit of data in the first floating gate;

storing a second bit of data in the second floating gate;

in a first read operation, reading the first bit of data; and

in a second read operation, reading the second bit of data.

39. (New) The method of Claim 38 wherein said act of storing a first bit of data comprises:

applying a positive voltage to the select gate;

applying a positive voltage to the second junction; and

applying ground potential or a positive voltage or a predesignated current to the first junction.

40. (New) The method of Claim 39 wherein said act of storing a second bit of data comprises:

applying a positive voltage to the select gate;

applying a positive voltage to the first junction; and

applying ground potential or a positive voltage or a predesignated current to the second junction.

41. (New) The method of Claim 40 wherein:

said act of storing a first bit of data further comprises applying ground potential to the body region, and

said act of storing a second bit of data further comprises applying ground potential to the body region.

42. (New) The method of Claim 40 wherein said positive voltage in said acts of applying a positive voltage to the select gate is about 3V, and said positive voltage in said acts of applying a positive voltage to the second junction and applying a positive voltage to the first junction is about 2.5V.

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43. (New) The method of Claim 38 wherein each of the first and second floating gates has at least one slanted surface forming a sharp edge so that insulating layer is thinnest between the sharp edge of each of the two floating gates and the select-gate.

44. (New) The method of Claim 39 wherein:

the act of applying ground potential or a positive voltage or a predesignated current to the first junction comprises:

forcing a predetermined amount of current through the channel region; and

measuring the voltage at the first junction, and

the act of applying ground potential or a positive voltage or a predesignated current to the second junction comprises:

forcing a predetermined amount of current through the channel region; and measuring the voltage at the second junction.

45. (New) The method of Claim 38 in combination with other similar cell structures forming a virtual ground array of rows and columns of cells, the cells along each row being serially connected, the select-gates of the cells along each row being connected together forming a plurality of horizontally-extending select-gate lines, the first junction of cells along each column of cells being connected together forming a first plurality of vertically-extending bitlines, and the second junction of the cells along each column of cells being connected together forming a second plurality of vertically-extending bitlines.

46. (New) A method of programming a memory cell having a source region and a drain region in a body region, the source and drain regions being separated by a channel region, the separation between the source and drain regions defining a cell channel length extending horizontally, each of the source and drain regions having a vertically-extending width, a horizontally-extending length, and a depth, the memory cell further having a first floating gate extending over a first portion of the channel region and overlapping the drain region, a second floating gate extending over a second portion of the channel region and overlapping the source region, and a select-gate extending over the first and second floating gates and extending across the entire length of each of the source and drain regions, the select gate being separated from the first and second floating gates only by an insulating layer, the method comprising:

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changing an electrical potential of the first floating gate by applying a first set of voltages to the select gate, the body region, the drain region, and the source region to induce injection of hot electrons into the first floating gate from the channel region under the source-side of the first floating gate; and

changing the electrical potential of the second floating gate by applying a second set of voltages to the select gate, the body region, the drain region, and the source region to induce injection of hot electrons into the second floating gate from the channel region under the drain-side of the second floating gate.

47. (New) The method of Claim 46 wherein:

said act of changing an electrical potential of the first floating gate comprises:

applying a positive voltage to each of the select gate and the drain region; and

applying a ground potential to each of the source and body regions, and

said act of changing an electrical potential of the second floating gate comprises:

applying a positive voltage to each of the select gate and source region; and

applying a ground potential to each of the drain and body regions.

48. (New) The method of Claim 46 wherein:

said act of applying a positive voltage to each of the select gate and the drain region comprises:

applying about 6.5V to the drain region; and

applying about 1.5V to the select gate, and

said act of applying a positive voltage to each of the select gate and the source region comprises:

applying about 6.5V to the source region; and

applying about 1.5V to the select gate.

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49. (New) The method of Claim 46 in combination with other similar cell structures forming a virtual ground array of rows and columns of cells, the cells along each row being serially connected, the select-gates of the cells along each row being connected together forming a plurality of horizontally-extending select-gate lines, the drain region of cells along each column of cells being connected together forming a first plurality of vertically-extending bitlines, and the source region of the cells along each column of cells being connected together forming a second plurality of vertically-extending bitlines.